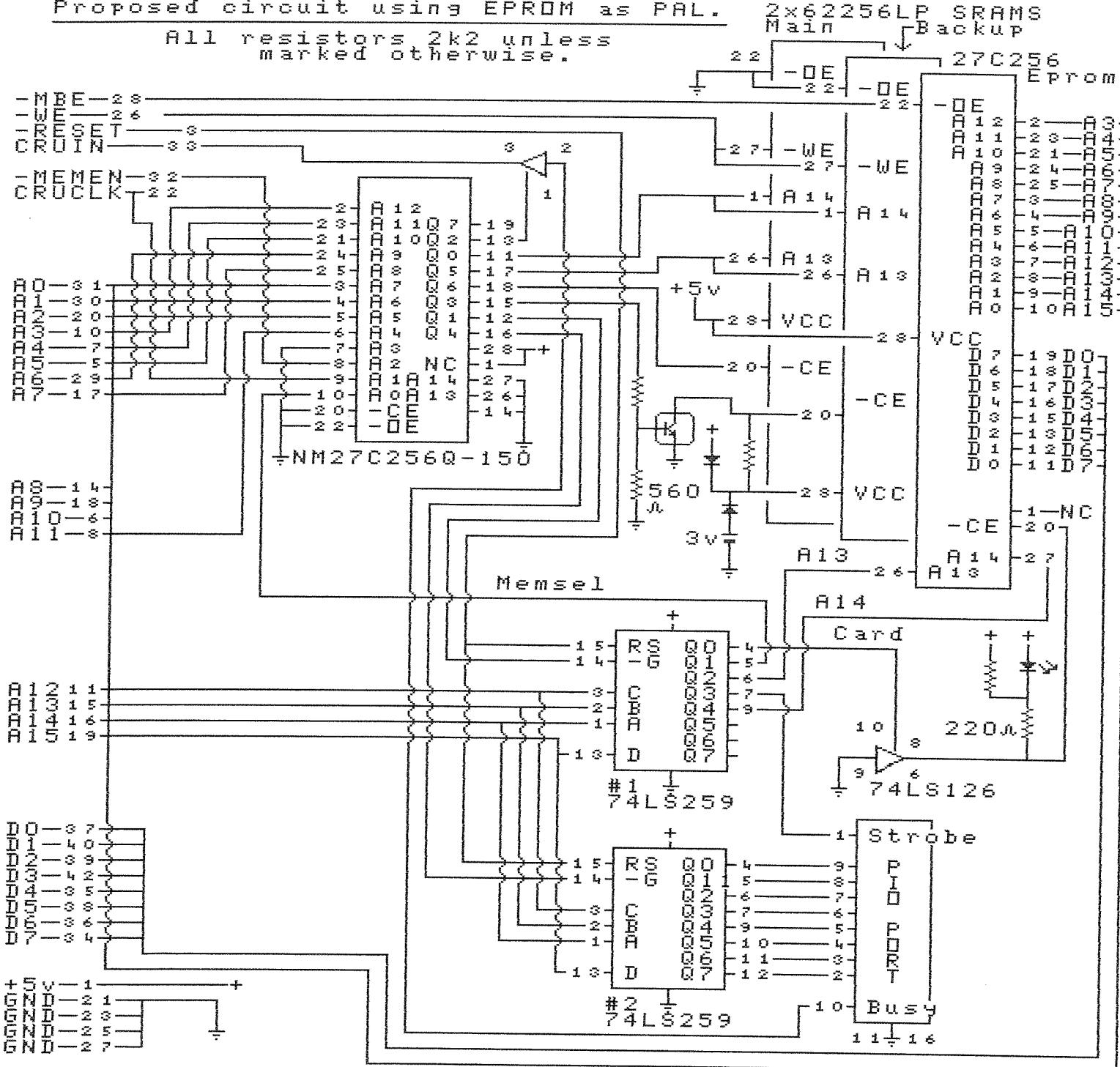


C A D E T Console Expansion Version 259PAC (C/GGT)

Proposed circuit using EEPROM as PAL - 2x62256LP SRAM

All resistors 2k2 unless
marked otherwise.



INPUTS

- Address bus (A₁₁ to A₀)
- Write enable (WE)
- Output enable (OE)
- Page address (PA₁ to PA₀)
- Page enable (PE)
- Chip select (CS)
- Program enable (PEN)
- Power supply (V_{CC}, V_{SS})
- Ground (GND)

OUTPUTS

- Data output (Q₁ to Q₀)
- Output enable (OE)
- Power supply (V_{CC}, V_{SS})
- Ground (GND)

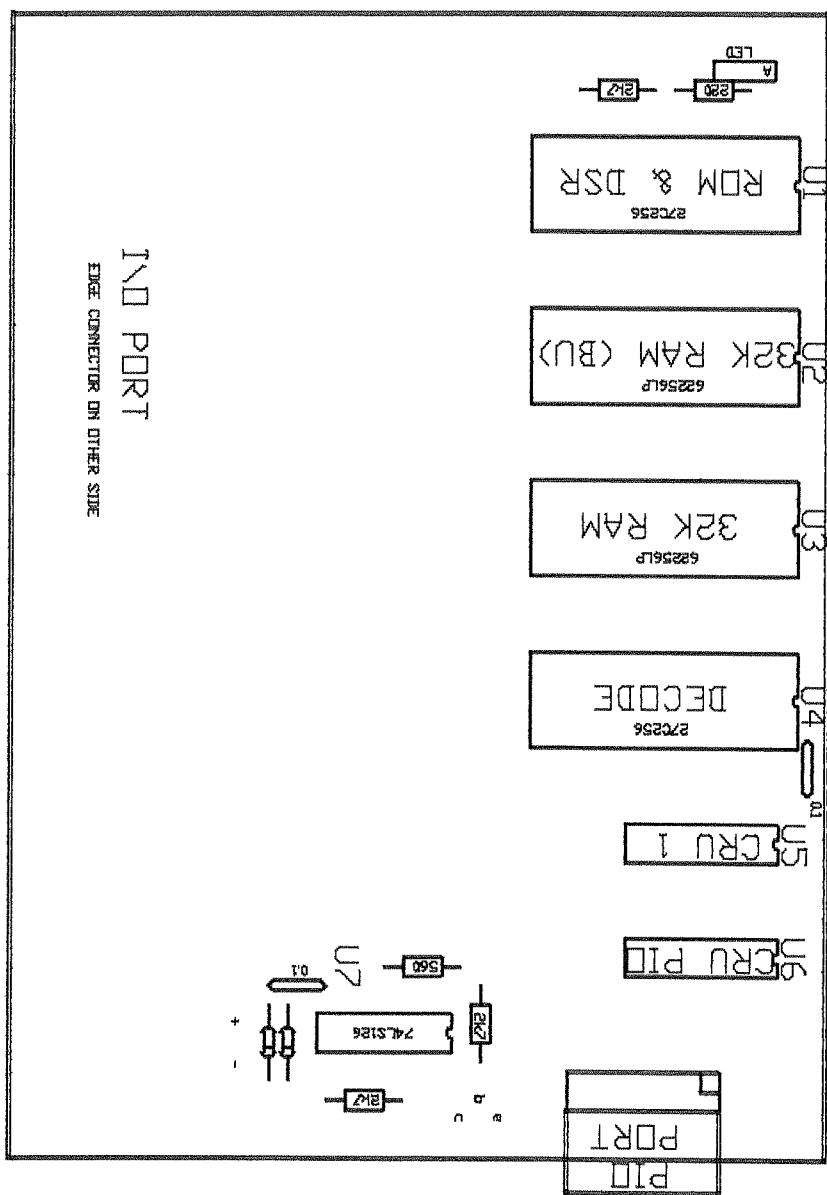
FUNCTIONS

- Addressing: Address bus (A₁₁ to A₀)
- Page selection: Page address (PA₁ to PA₀)
- Output enable: Output enable (OE)
- Program enable: Program enable (PEN)
- Power supply: Power supply (V_{CC}, V_{SS})
- Ground: Ground (GND)

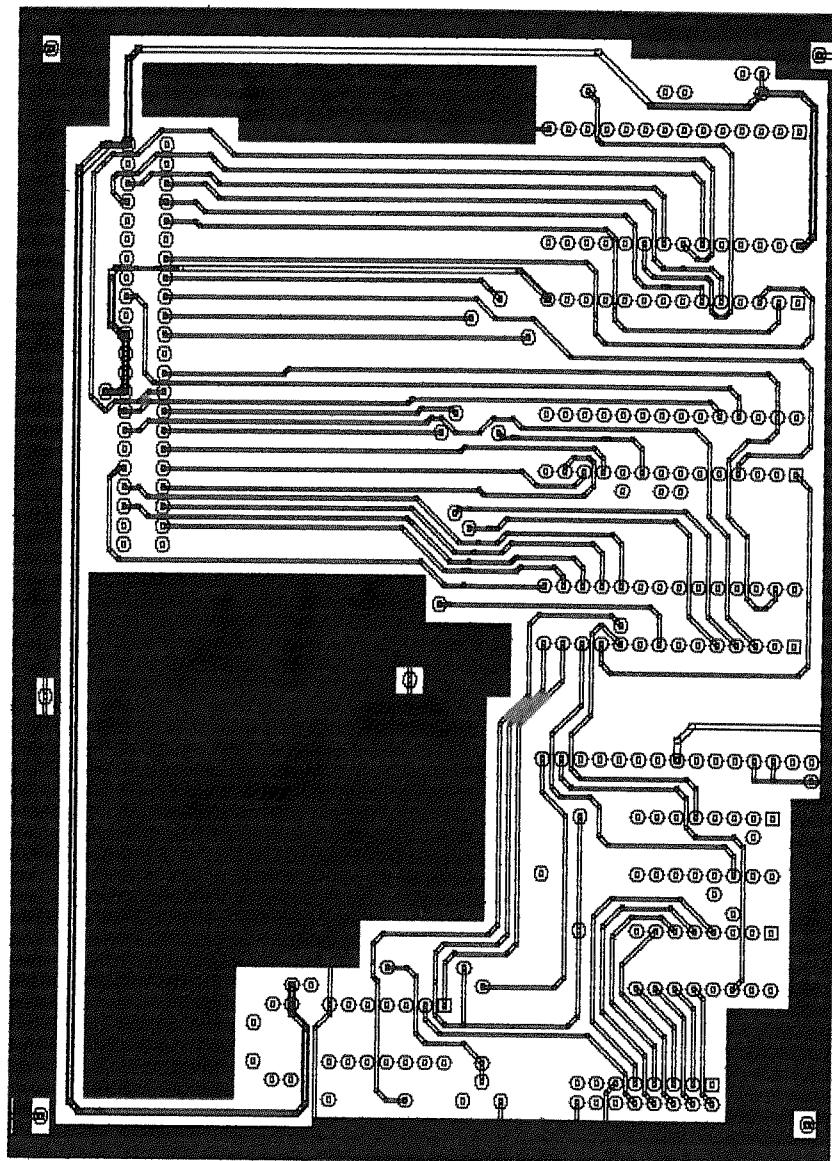
VALID ADDRESSING

The diagram shows the connection of the address bus (A₁₁ to A₀) to the NM27C256Q-150 chip. The address bus is connected to the address pins of the chip. The page address (PA₁ to PA₀) is also connected to the chip. The output enable (OE) is connected to the OE pin of the chip. The program enable (PEN) is connected to the PEN pin of the chip. The power supply (V_{CC}, V_{SS}) and ground (GND) are also connected to the chip.

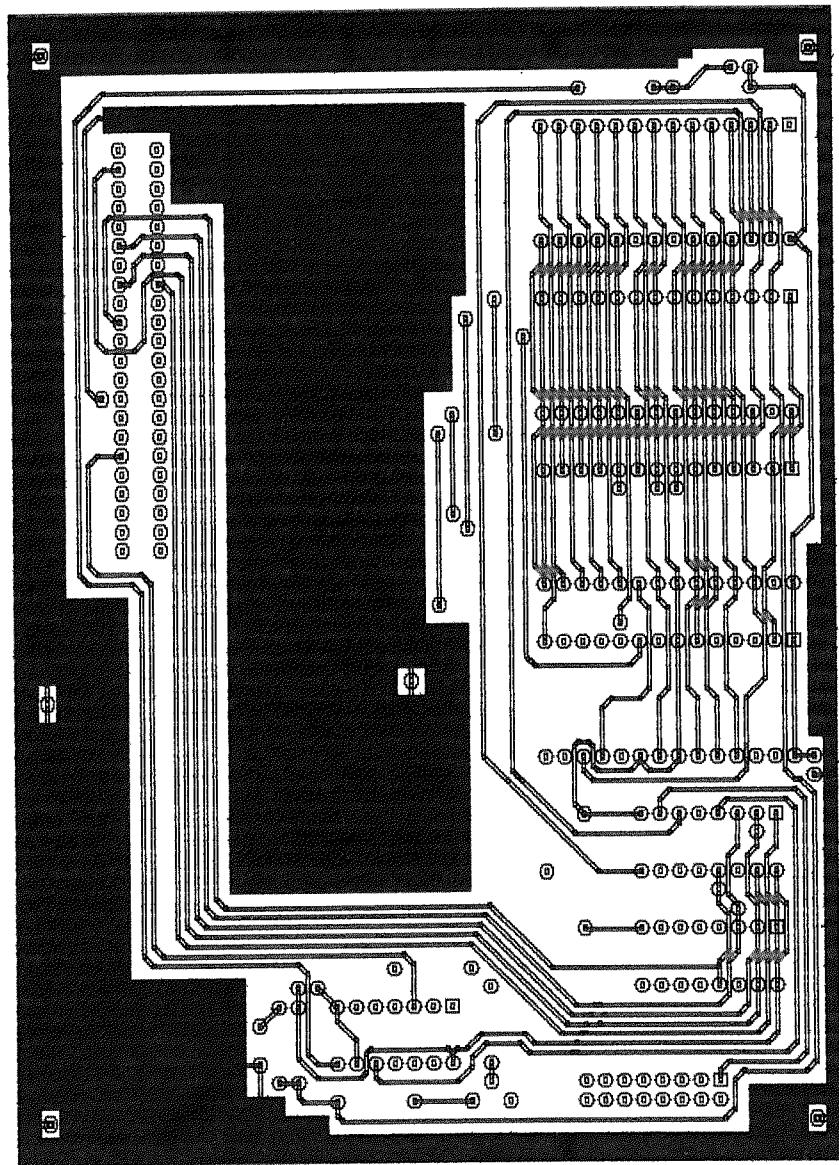
CADET Overlay

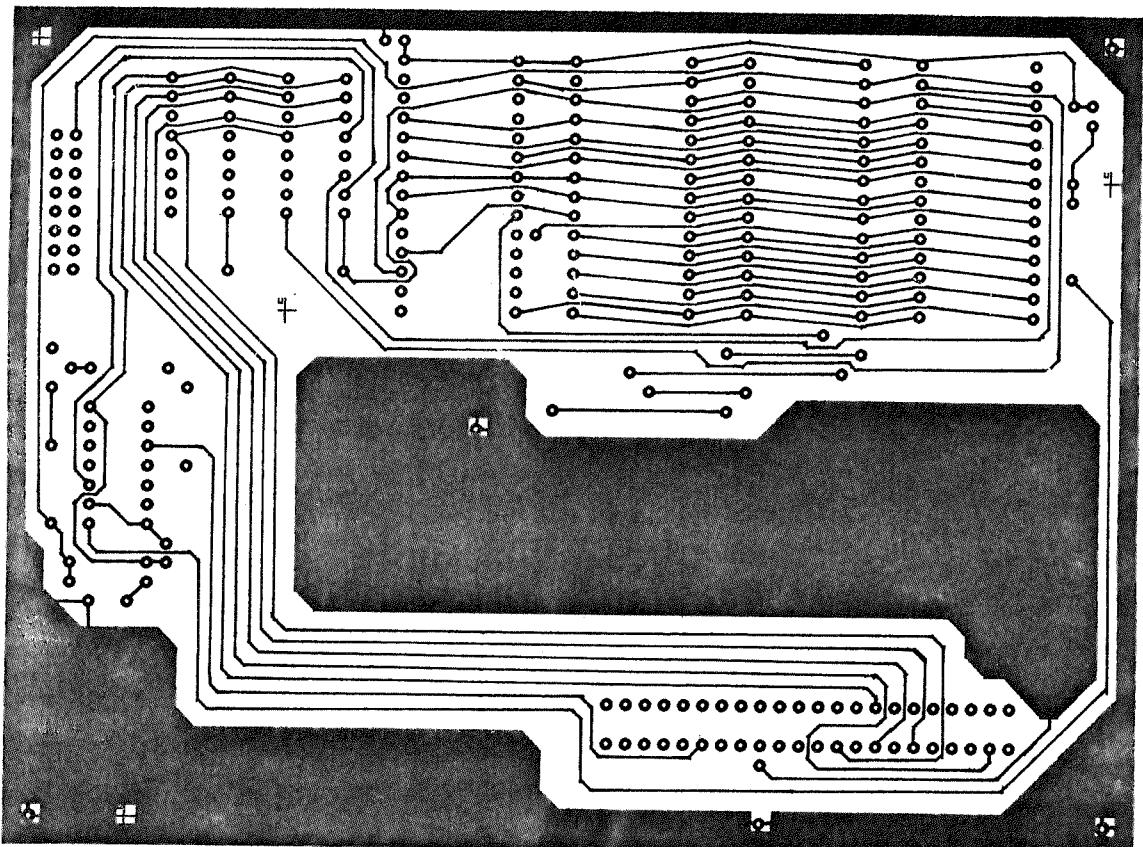
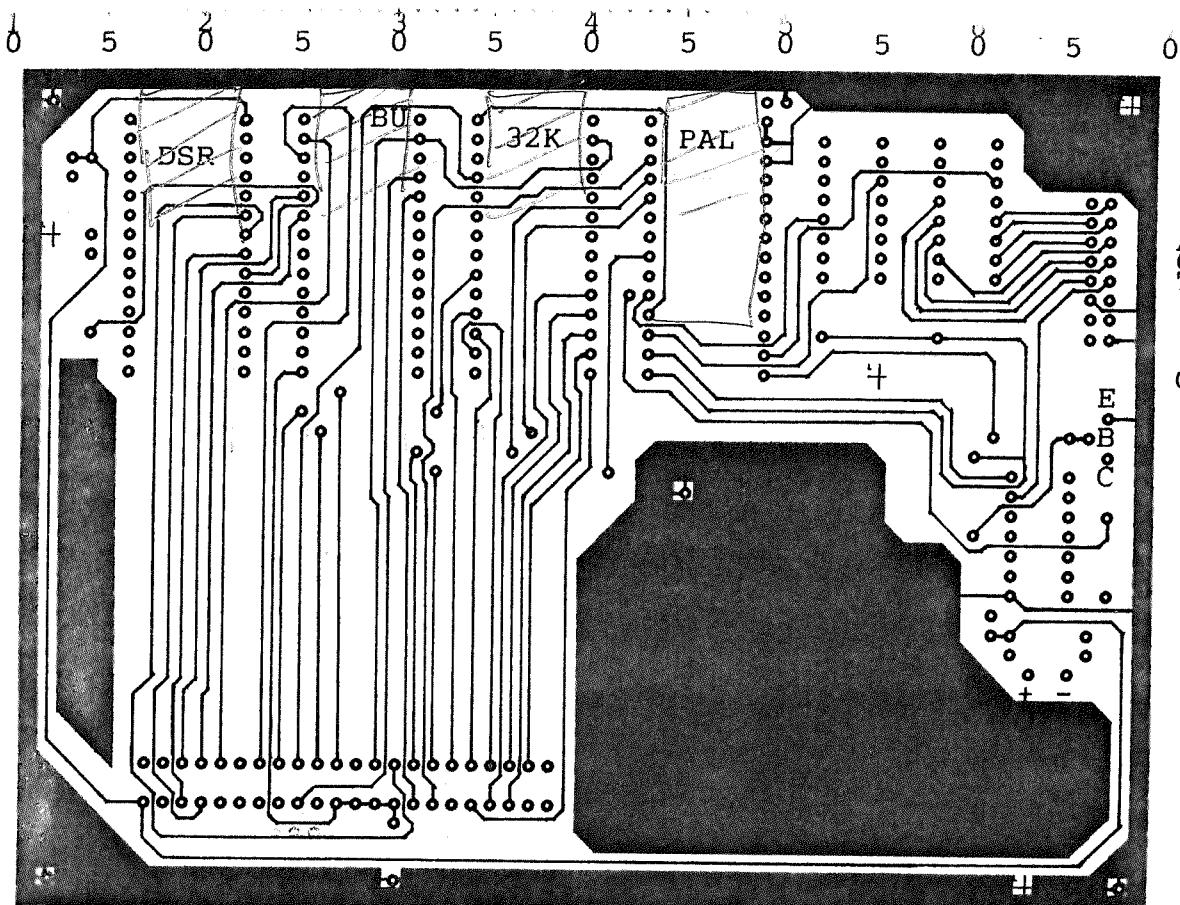


CADET Top Layer



CADET Bottom Layer





TAIKOR "PAL" pins 26, 27, 1 according to EPROM type.

27C256 both to ground

27C128 Pin 26 to ground, Pin 27 to + NOTE PCB shows

27C64 Pin 26 NC Pin 27 to + Pin 27 to both GND and to +

~~4x~~ Jumper Wires

74LS259 Pin 1 to RAMs pin 9

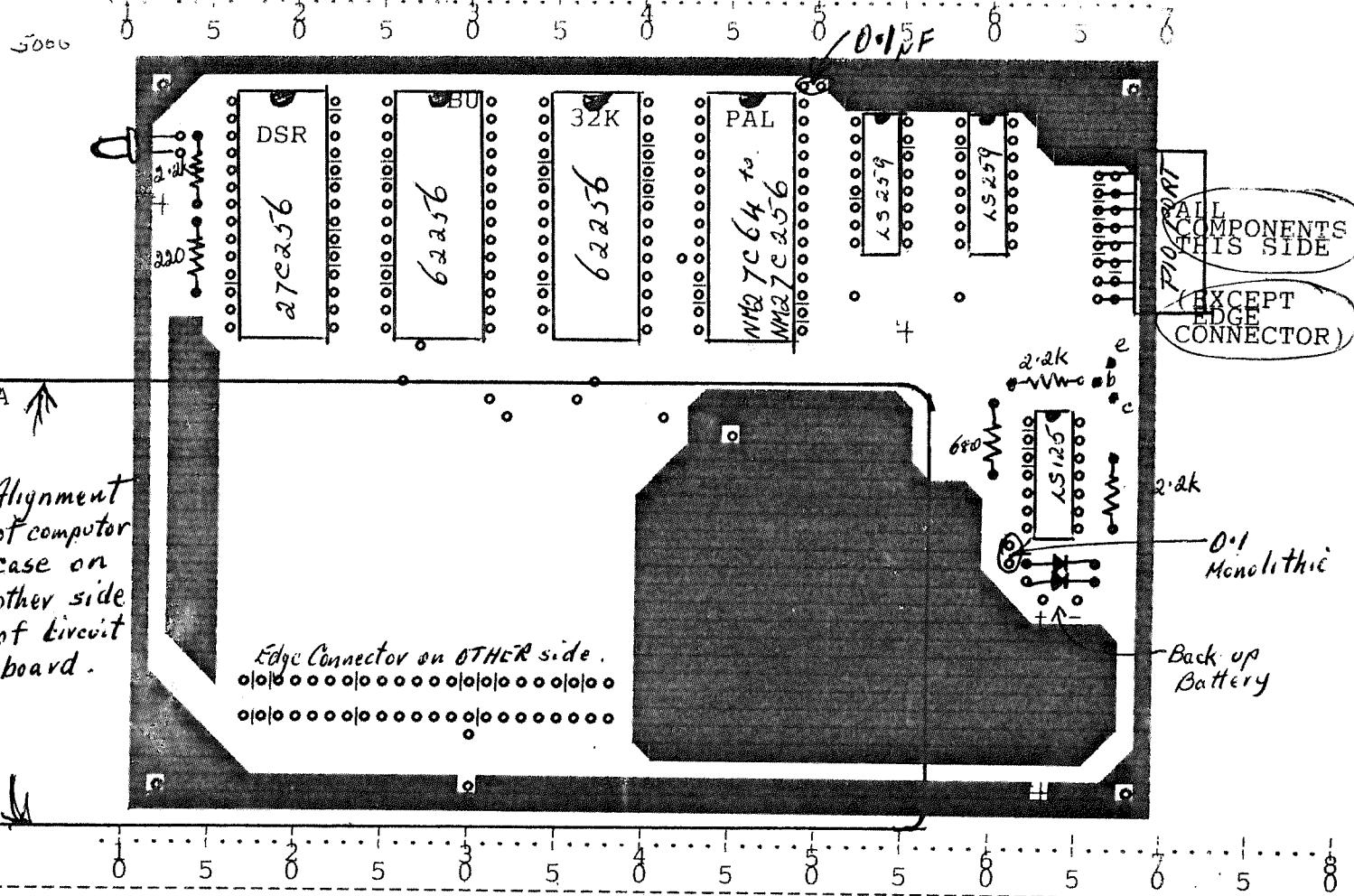
" Pin 2 to " pin 8

" Pin 3 to " pin 7

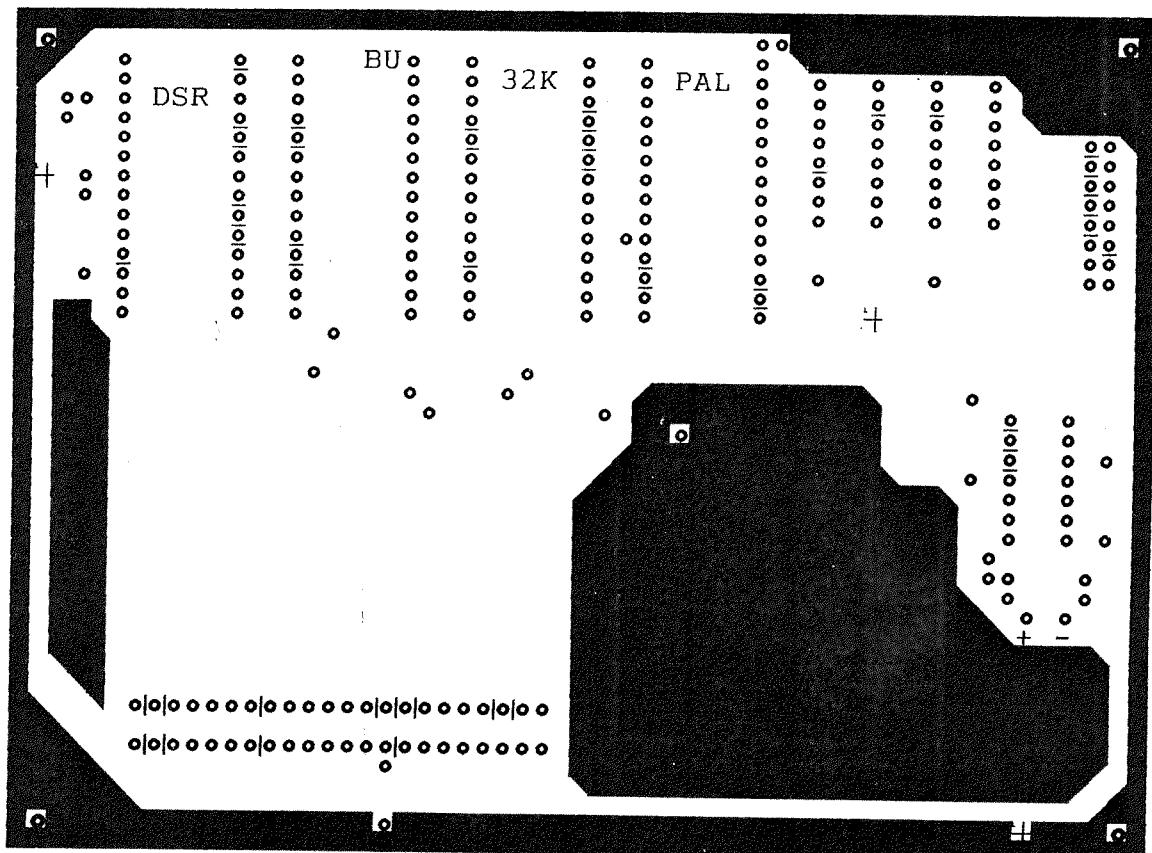
" Pin 13 to " pin 10

{FILE C2PCBFLAT}

8/01



(FILE C2PCBFLAT)



~~ALL
COMPONENTS
THIS SIDE~~

(EXCEPT
EDGE
CONNECTOR)

